MITEL
SEMICONDUCTOR

NWK954

QUAD FAST ETHERNET REPEATER

PRELIMINARY INFORMATION

Supersedes January 1998 version, DS4842 - 1.1

DS4842-2.1 April 1998

The NWK954 is a fully integrated, unmanaged, 4-port Fast Ethernet Repeater conforming to the IEEE 802.3 100BASE-TX Standard. The device integrates the 802.3 Repeater functions with four 100BASE-TX PHY modules, enabling direct connection to the isolation transformers with no additional PHY components.

It has built-in LED drivers for display of port activity and network utilization. There is a local expansion port which allows up to six NWK954s to be cascaded to form a 24-port repeater with no additional components.

With the addition of simple backplane driver/receivers, up to eight 24-port repeaters can be stacked.

The NWK954 is supplied in a 128-pin PQFP and interfaces to the twisted pair media through 1:1 isolation transformers.

ORDERING INFORMATION

NWK954D/CG/GH1N

FEATURES

- Compliant with IEEE 802.3 100BASE-TX Repeater Unit Specification
- Incorporates four IEEE 802.3 Compliant 100BASE-TX Ports
- Local Expansion Port for Cascading to 24 Ports
- Stackable Backplane for Expansion up to 192 Ports
- Link/Activity LED and Receive Error LED for each Port
- Collision LED
- Five LED Network Utilization Display
- Base Line Wander Correction
- Power Saving on Unused Ports
- Driven from a Single 25MHz Clock
- Single 5V supply
- Low Power CMOS Technology
- 128-pin PQFP package

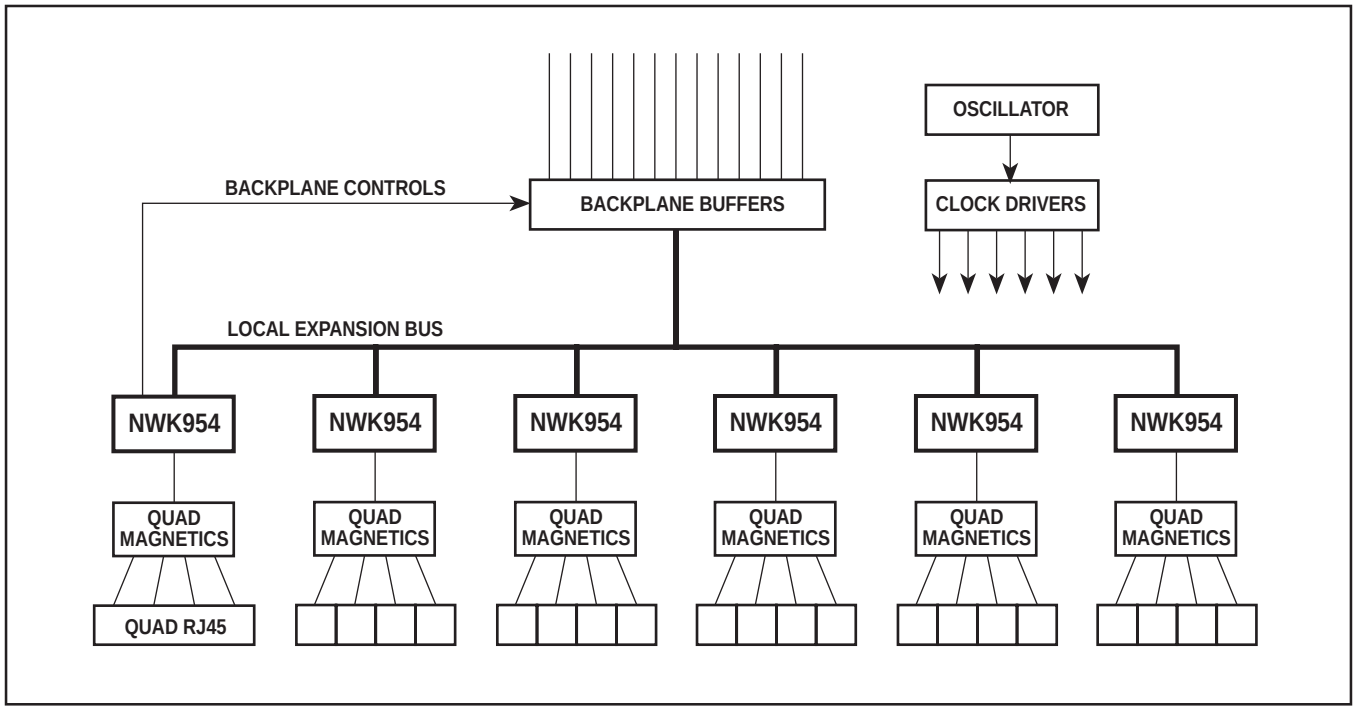

Fig. 1 System block diagram

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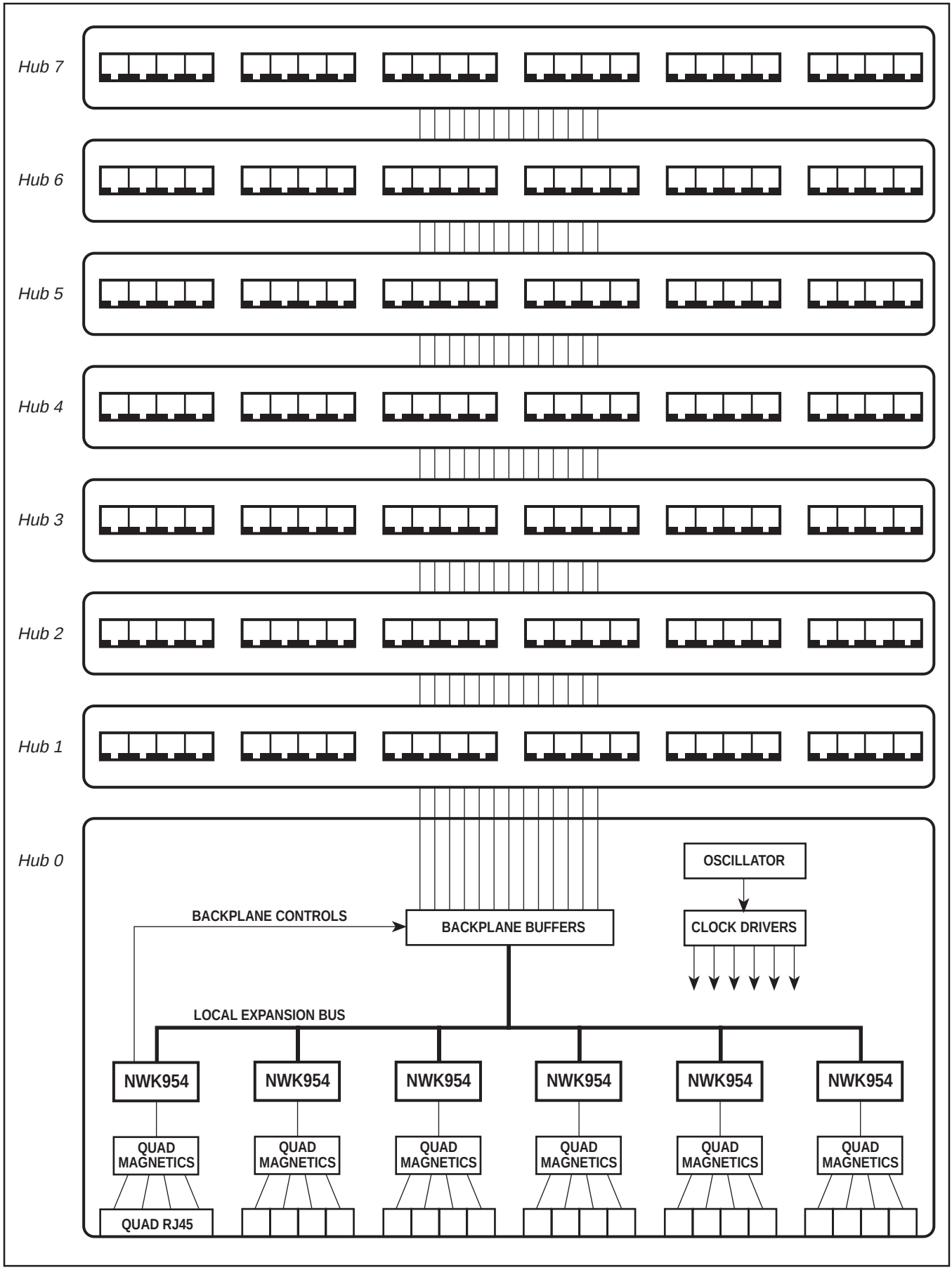

Fig. 2 192-port stacked repeater

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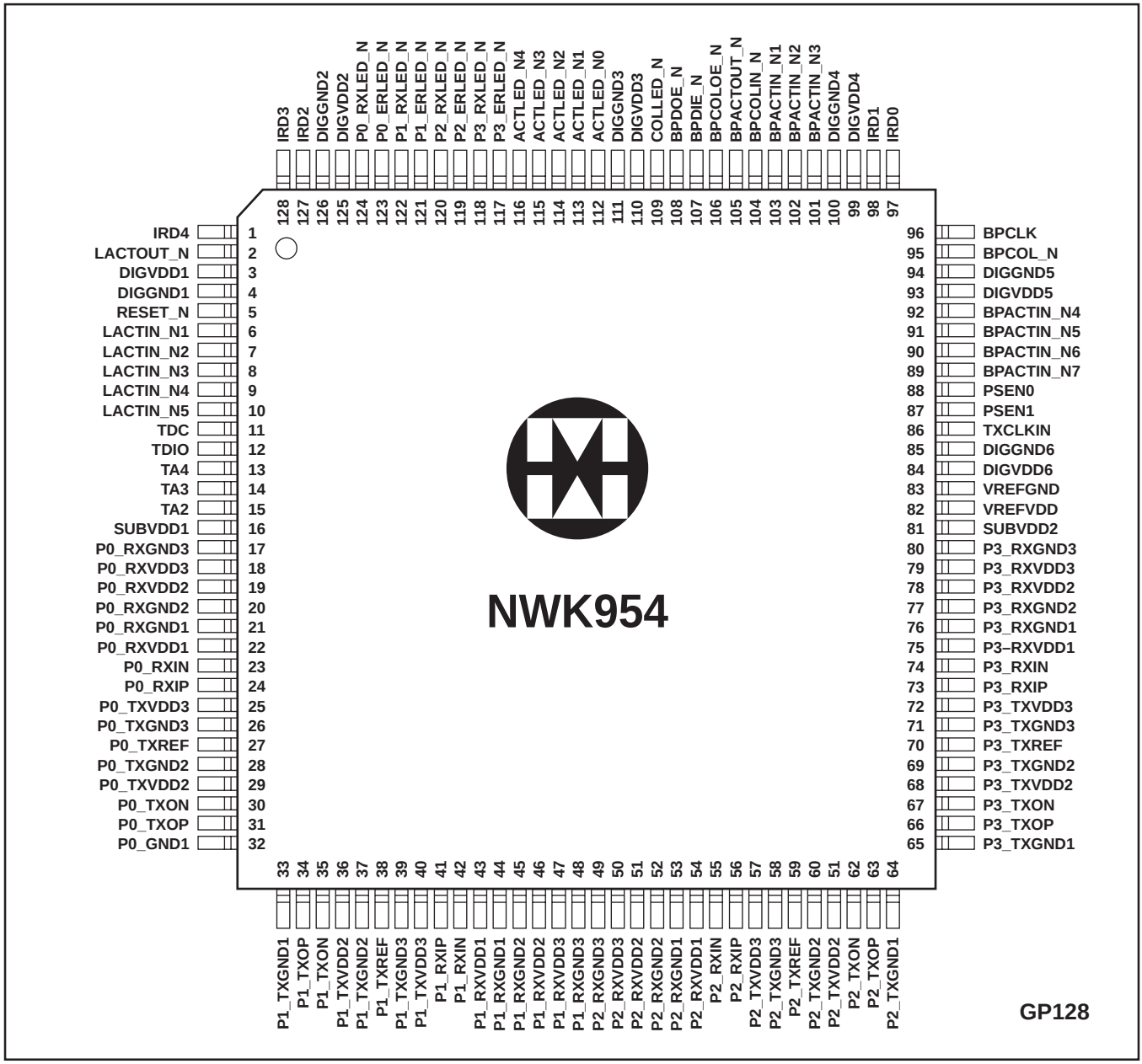

Fig. 3 Pin connections – top view

FUNCTIONAL DESCRIPTION

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The NWK954 is a mixed-signal CMOS device which integrates all of the functions required for an unmanaged 4-port 100BASE TX repeater as defined in the IEEE 802.3 Standard. The device incorporates all of the necessary 100BASE-TX PHY functions to allow direct interfacing to a quad 1:1 magnetics module with a modest number of external passive components. The built-in expansion port allows cascading of up to 6 NWK954s to build a 24-port repeater with no additional components and also allows stacking of up to eight 24-port repeaters with the addition of simple backplane driver/receiver components. The operating status of the device is indicated on 14 outputs designed to directly drive LEDs. This high level of integration combined with low power consumption and low pin count offers an efficient and low cost solution for Fast Ethernet unmanaged repeater design.

Compliance with Standards

The NWK954 is designed for compliance with the IEEE 802.3 Standard, Clause 24 (100BASE-X PCS and PMA), Clause 25 (100BASE-TX PMD) and Clause 27 (Repeater for 100Mb/s Baseband Networks). Clause 25 references the FDDI twisted pair PMD Standard, henceforth referred to as TP-PMD.

Compatibility With Other Devices

The NWK954 is designed to connect directly to 5 other NWK954 devices using the expansion bus. The Expansion Port is identical to that used on the NWK950 Repeater Controller. The Expansion Port may be connected to a backplane through external driver/receivers. The backplane specification is identical to that used by the NWK950, so repeaters using the NWK950 may be stacked with repeaters using the NWK954.

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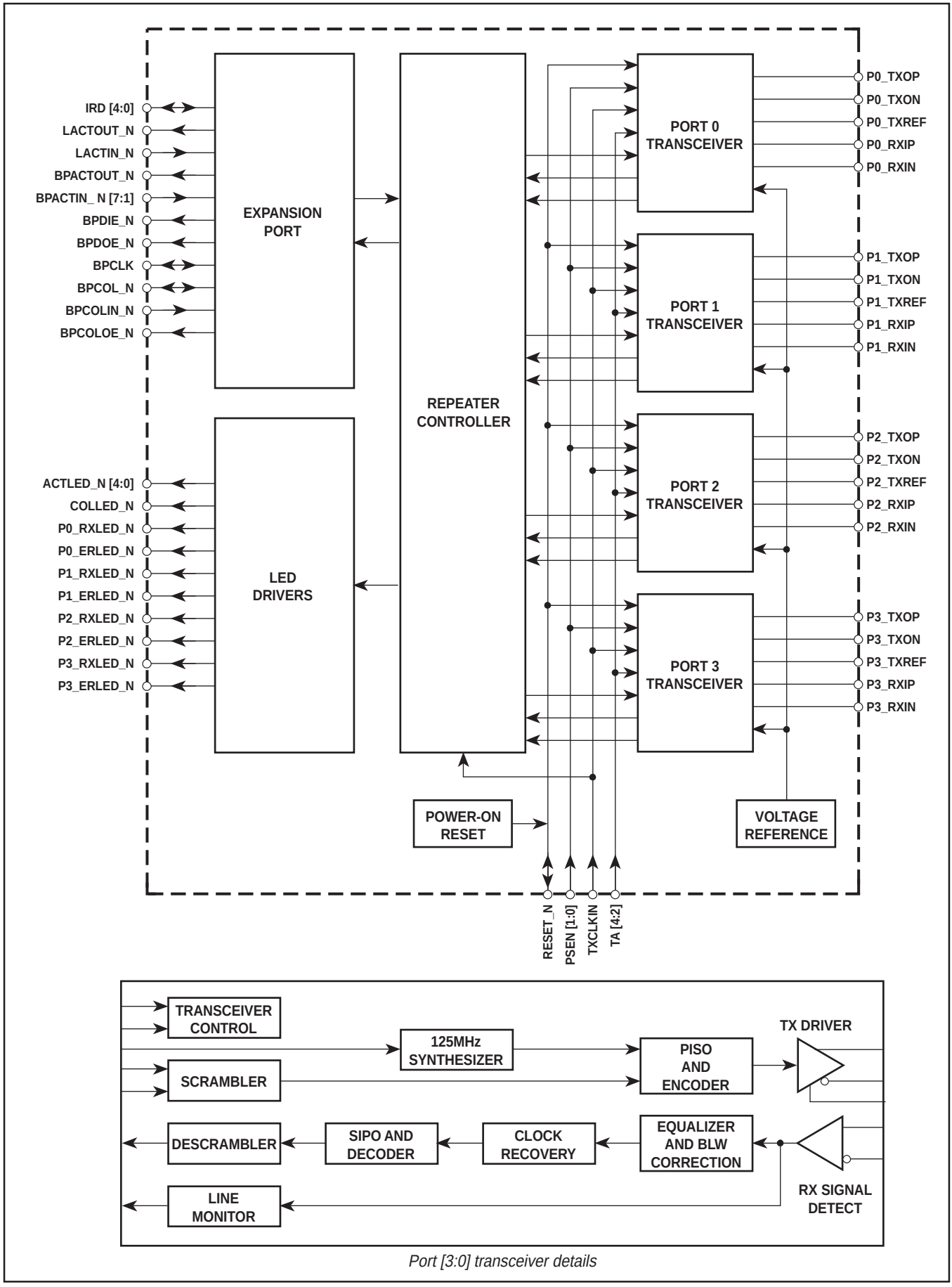

Port [3:0] transceiver details

Fig. 4 NWK954 block diagram

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Basic Repeater Function

The Repeater Controller monitors activity on the 4 twisted pair ports and on the Expansion Port. When a packet is received on one of the twisted pair ports it is forwarded to the other 3 twisted pair ports and to the Expansion Port. When a packet is received on the Expansion Port it is forwarded to all 4 twisted pair ports. When receive activity is detected on 2 or more ports the Repeater Controller will send the jam signal to all twisted pair ports for the duration of all activity associated with the collision event.

Jabber Protection

The Repeater Controller provides receive jabber protection to ensure that the network is not disrupted by excessively long data streams. If a received data stream exceeds 65,536 bit times then the receiving port will be shutdown. In the shutdown state data received on the faulty port is ignored and packets received from other ports are not transmitted to the faulty port. A port will recover from the shutdown state when the incoming data stream ends or if the device is reset.

Auto-Partition Function

The auto-partition function prevents faulty behaviour on a network segment from disrupting the entire network. The Repeater Controller counts consecutive collisions on each port and will partition a port that causes more than 60 consecutive collisions. In the partitioned state, packets received on the faulty port will be ignored but packets received from other ports will continue to be transmitted to the faulty port. The port will recover from the partitioned state when valid activity is detected on the port or if the device is reset.

Carrier Integrity Monitor

The Repeater Controller detects false carrier events on all ports. A false carrier is defined as receive activity that does not commence with the correct start-of-packet sequence. When a false carrier event is detected, the Repeater Controller will transmit the jam signal on all ports for the duration of the false carrier event provided it does not exceed 450-500 bit times. After this time the port will be isolated and the jam signal will cease. The NWK954 will also isolate a port that suffers 2 successive false carrier events. In the isolated state, packets received from the faulty port are ignored and packets received from other ports are not transmitted to the faulty port. A port will recover from the isolated state when a valid inter-packet gap is detected and is followed by either a valid packet exceeding 450-500 bit times or by an idle sequence exceeding 33000 (±25%) bit times.

Expansion Port

The Expansion Port allows up to 6 NWK954s to be cascaded. This allows a 24-port hub to be built with no additional external components. The Expansion Port includes a 5-bit parallel bidirectional data bus (IRD) which carries unscrambled symbol data and a 25MHz sampling clock (BPCLK). Each NWK954 indicates receive activity on any of its 4 twisted pair ports by asserting the local activity output (LACTOUT_N). The LACTOUT_N signals from each NWK954 connect to the local activity inputs (LACTIN_N) of all the other cascaded NWK954s.

When a collision occurs between 2 twisted pair ports on an NWK954, the event is communicated to other cascaded NWK954s by asserting the collision signal (BPCOL_N). This instructs all cascaded NWK954s to transmit the jam signal for the duration of the collision event. BPCOL_N is also asserted when a collision occurs between 2 twisted pair ports on different NWK954s.

Backplane

The Expansion Port allows hubs to be stacked via a backplane bus. This requires the addition of some simple external driver/ receivers. The functional requirement for these components is illustrated in Fig. 6. Contact Mitel for full details of recommended components.

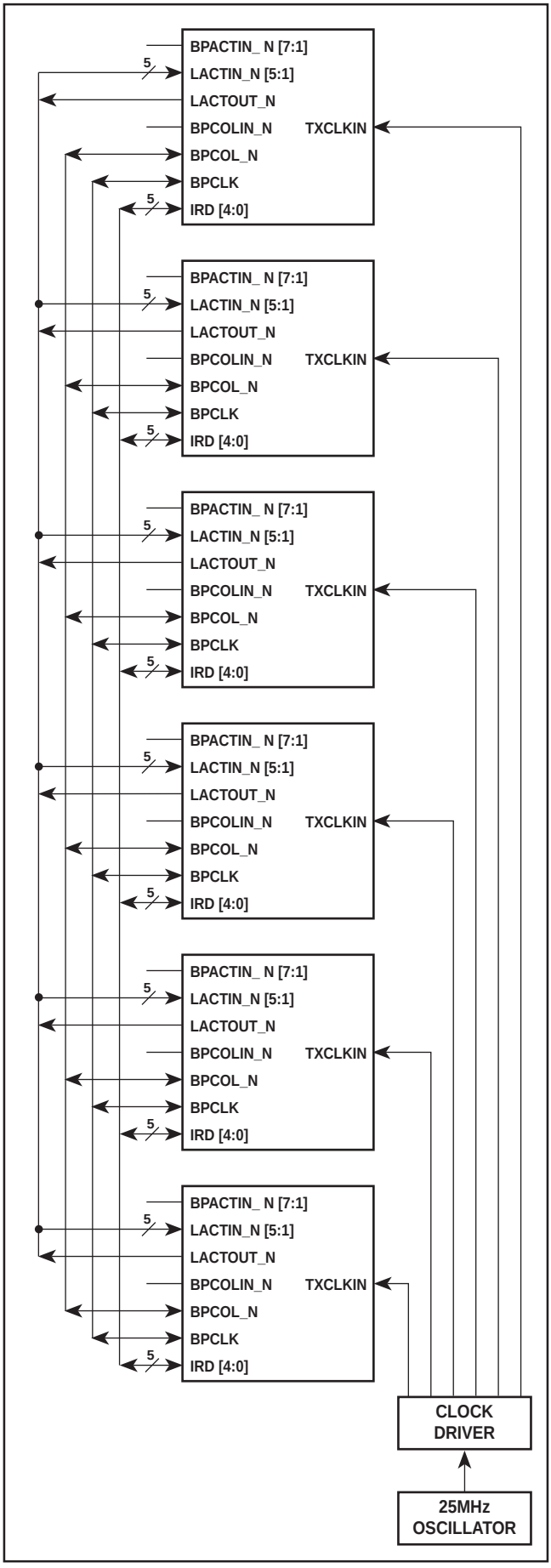

Fig. 5 Cascaded NWK954s

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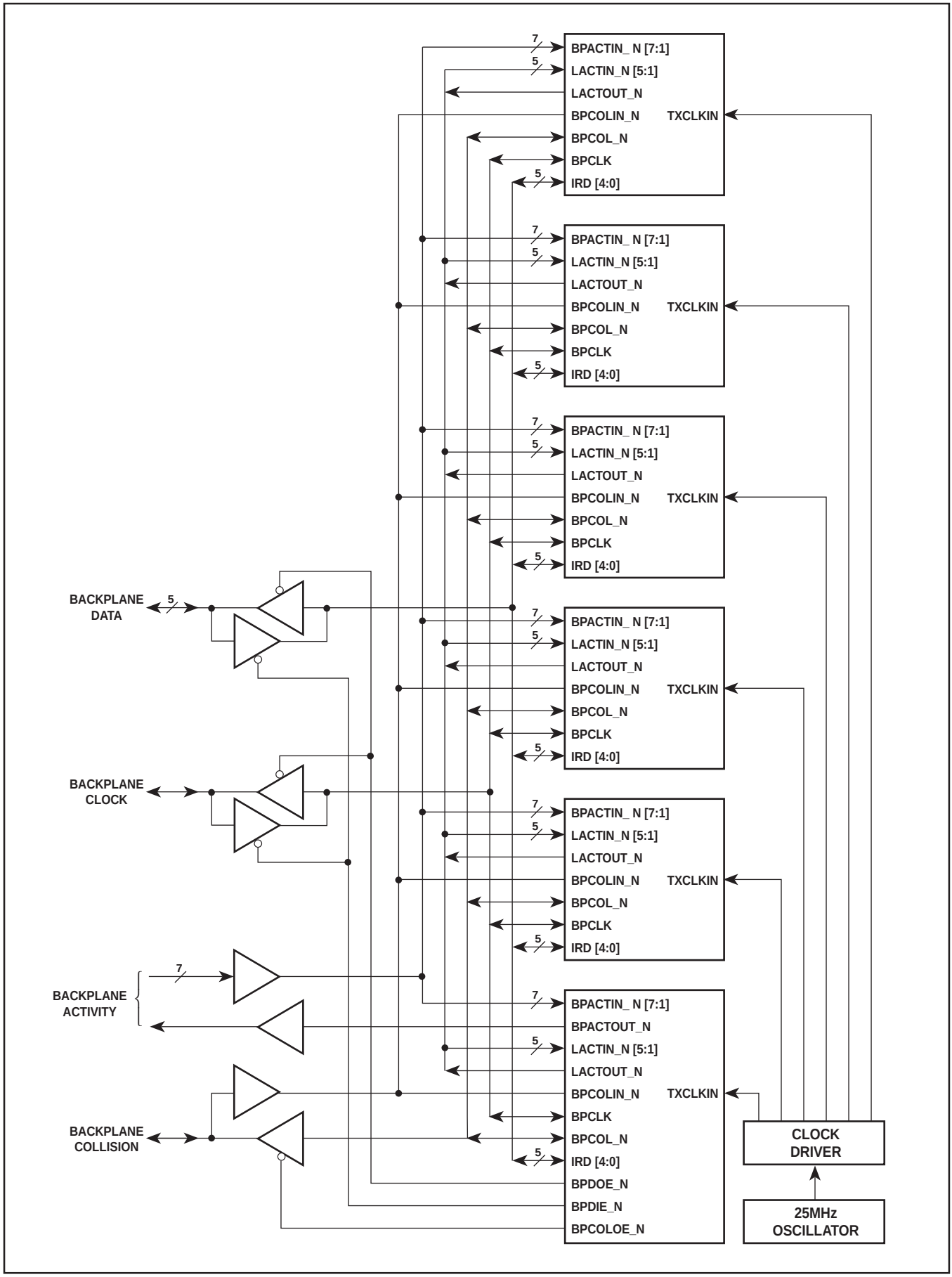

Fig. 6 External backplane drivers/receivers

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The IRD bus in each hub is connected to the 5-bit backplane bus via a bidirectional buffer. This allows data to be driven from any hub to all other hubs in the stack. The bidirectional buffer is controlled by 2 control signals (BPDOE_N and BPDIE_N) which can be taken from any one of the NWK954 devices in the hub. BPDOE_N and BPDIE_N default to being active low but can be independently changed to active high by the addition of an external pull-down resistor, as shown in Fig.7. This resistor is sensed during RESET_N = 0.

Data transfers on the backplane are synchronous to the backplane clock. The backplane clock is supplied by whichever hub supplies the data. When receiving data from the backplane, the backplane clock is enabled onto the local BPCLK signal by BPDIE_N. BPCLK connects to all NWK954s in the hub. When a hub supplies data to the backplane, BPCLK is driven locally and is enabled onto the backplane by BPDOE_N.

Each hub in a stack indicates receive activity on any of its twisted pair ports by asserting the backplane activity output (BPACTOUT_N). BPACTOUT_N can be taken from any one of the NWK954s and drives one of the backplane activity signals via an external buffer. The backplane supports up to 8 backplane activity signals. The backplane activity signals from up to 7 other hubs connect to the local BPACTIN_N signals which are input to all NWK954s in the hub.

When a collision occurs between 2 twisted pair ports in a hub, the event is communicated to other stacked hubs by BPCOL_N which is enabled onto the backplane collision signal by BPCOLOE_N. BPCOLOE_N defaults to being active low but can be changed to active high by the addition of an external pull-down resistor. This resistor is sensed during RESET_N=0. BPCOL_N is also asserted when a collision occurs between two twisted pair ports on different hubs. Collision events are cormmunicated to all hubs through the BPCOLIN_N signal which connects to all NWK954s in the hub.

LED Drivers

The NWK954 provides 2 LED drivers per port to indicate port status (RXLED_N and ERLED_N), one LED driver to indicate collisions (COLLED_N) and 5 LED drivers to indicate network utilization (ACTLED_N). The LED drivers pull the output pins low to turn the LEDs on. The LEDs are turned on or off for a minimum of 40ms to ensure observability.

The port status LEDs indicate a variety of conditions and provide rapid diagnosis of network faults,as shown in Table 1. The network utilization LEDs are turned on at the thresholds given in Table 2.

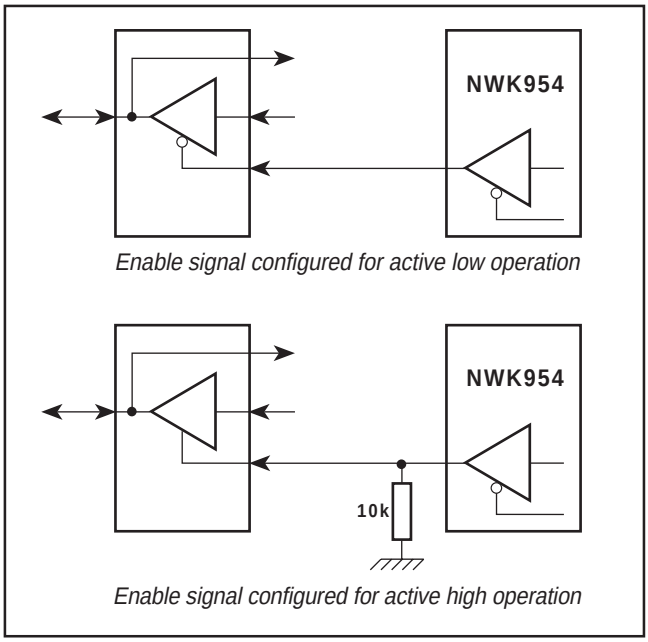

Fig. 7 Polarity selection on BPDOE_N, BPDIE_N and BPCOLOE_N

RXLED_N	ERLED_N	Port status
Off	Off	No incoming signal
Off	Flash	Incoming signal but no idle pattern recognized*
On	Off	Link established, no incoming data packets
Flash	Off	Link established, receiving data packets
On	On	Link established, but port partitioned due to excessive collisions or port isolated due to false carriers or port disabled due to jabber
Flash off	Flash on	Link established, false carrier or invalid data detected

* In 802.3 a continuous signal of the required amplitude is sufficient to establish a link but no data can be passed to the repeater controller until the descrambler has locked on to an idle pattern.

Table 1

LED	Network utilization
ACTLED_N0	>1%
ACTLED_N1	>12·5%
ACTLED_N2	>25%
ACTLED_N3	>50%
ACTLED_N4	>60%

Table 2

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100BASE-TX Receiver

The 100BASE-TX receiver recovers data from up to 140m of Cat5 UTP cable. Received data is decoded and descrambled and presented to the repeater controller as 5-bit symbols. The Transceiver Controller sequences the start-up of the receiver and does not allow data to be passed to the Repeater Controller until the receiver is fully initialized and a link is established and the descrambler is synchronized. After start-up the Transceiver Controller monitors the receiver and takes corrective action if a fault is detected.

The Signal Detect continuously monitors the level on the RXIP/RXIN differential input and indicates to the Transceiver Controller when the signal amplitude is within the range of the Equalizer. The acceptable level is considerably less than that specified in the 802.3 Standard because the NWK954 receiver is designed for recovery of signals from up to 140m of Cat5 UTP cable.

The Equalizer compensates for the signal attenuation and distortion resulting from transmission down the cable and through the isolation transformers. The Equalizer self- adjusts within 1ms of Signal Detect indicating that the incoming signal is within the acceptable range. Thereafter the Equalizer continuously adjusts to small variations in signal level without corrupting the received data.

The 100BASE-TX MLT3 code contains significant low frequency components which are not passed through the isolation transformers and cannot be restored by the Equalizer. This leads to a phenomenon known as baseline wander (BLW) which will cause an unacceptable increase in error rate if not corrected. The NWK954 employs a quantized feedback technique to restore the low frequency components and thus maintain a very low error rate even when receiving signals such as the 'killer packet' described in the TP-PMD specification.

The Clock Recovery circuit uses a Phase-Locked Loop (PLL) to derive a sampling clock from the incoming signal. The recovered clock runs at the symbol bit rate (nominally 125MHz) and is used to clock the MLT3 decoder and the Serial-to-Parallel converter (SIPO). The recovered clock is divided by 5 to generate the receive clock which is used to strobe received data into the Repeater Controller. The Transceiver Controller monitors behaviour of the PLL and re-initializes the receiver if lock is lost.

The SIPO and Decoder convert the received signal from serial MLT3 to 5-bit parallel NRZ.

The Link Monitor implements the 802.3 Link Monitor State Machine which indicates when a sustained signal of appropriate quality and amplitude is being received. This is the first stage in establishing a link; no data can be passed to the Repeater Controller until the Descrambler is synchronized to the incoming signal. Descrambler synchronization is established during reception of the idle pattern. After synchronization is established, the Descrambler output is continuously monitored and the Descrambler is re-synchronized if insufficient idle sequences are detected.

100BASE-TX Transmitter

The 100BASE-TX transmitter generates a 125MHz transmit clock and uses it to serialize and transmit the 5-bit symbol data input from the Repeater Controller. The Transceiver Controller sequences the start-up of the transmitter and does not allow transmission onto the twisted pair until the transmitter is fully initialized. After start-up the Transceiver Controller monitors the transmitter and takes corrective action if a fault is detected.

The Scrambler mixes the symbol data with a 2047-bit pseudo-random code, in accordance with the TP-PMD Standard. The four Scramblers in the NWK954 are seeded with different values based on the TA[4:2] input. When multiple NWK954s are cascaded to make a hub, each NWK954 should have a unique value on TA[4:2] to ensure that all of the Scramblers in the hub are seeded with different values.

The 125MHz Synthesizer employs a phase-locked loop (PLL) to generate a 125MHz timing reference from the 25MHz reference clock. The Transceiver Controller monitors behaviour of the PLL and re-initializes the Synthesizer if lock is lost.

The PISO and Encoder take NRZ-coded symbols from the Scrambler, and convert them to serial MLT3 for outputting to the TX Driver. The PISO and Encoder do not operate until the 125MHz Synthesizer is locked to the 25MHz reference. This avoids transmission of spurious signals onto the twisted pair.

The TX Driver outputs the differential signal onto the TXOP and TXON pins. It operates with 1:1 magnetics to provide impedance matching and amplification of the signal in accordance with the 802.3 specifications. The transmit current is governed by the current through the TXREF100 pin, which must be grounded through a resistor as described in Table 10.

Power Saving on unused ports

The NWK954 incorporates a feature that will automatically shutdown the transceivers on unused ports. The shutdown occurs if Signal Detect indicates that no signal has been received for 2·5s. The transceiver is re-started when Signal Detect indicates that an incoming signal has been detected. This feature is intended to save power and reduce noise in unconnected ports. In certain circumstances, such as in port-to-port links between hubs, this feature should be suppressed by appropriate setting of the PSEN [1:0] inputs, as shown in Table 3.

Initialization

The NWK954 incorporates a power-on reset circuit for self-initialization on power-up. During power-on reset the open drain RESET_N pin is driven low. It will not normally be necessary for the user to drive RESET_N because the NWK954 is designed to automatically recover from fault conditions; however, if required, the user may initialize the device by pulsing RESET_N low.

PSEN1	PSEN0	Function
0	0	Power saving disabled on all ports
0	1	Power saving enabled on ports 1, 2 and 3, disabled on port 0
1	0	Power saving enabled on ports 0, 1 and 2, disabled on port 3
1	1	Power saving enabled on all ports

Table 3 Power saving functions

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PIN DESCRIPTIONS

Active low signals are denoted by the _N suffix; all other signals are active high

Network Interface

Signal	Pin no.	Type	Description
P0_RXIP	24	Analog input	(+) Differential receive signal from port 0 magnetics
P0_RXIN	23	Analog input	(−) Differential receive signal from port 0 magnetics
P0_TXOP	31	Analog output	(+) Differential transmit signal to port 0 magnetics
P0_TXON	30	Analog output	(−) Differential transmit signal to port 0 magnetics
P0_TXREF	27	Analog output	Port 0 transmitter current setting pin, grounded externally
P1_RXIP	41	Analog input	(+) Differential receive signal from port 1 magnetics
P1_RXIN	42	Analog input	(−) Differential receive signal from port 1 magnetics
P1_TXOP	34	Analog output	(+) Differential transmit signal to port 1 magnetics
P1_TXON	35	Analog output	(−) Differential transmit signal to port 1 magnetics
P1_TXREF	38	Analog output	Port 1 transmitter current setting pin, grounded extemally
P2_RXIP	56	Analog input	(+) Differential receive signal from port 2 magnetics
P2_RXIN	55	Analog input	(−) Differential receive signal from port 2 magnetics
P2_TXOP	63	Analog output	(+) Differential transmit signal to port 2 magnetics
P2_TXON	62	Analog output	(−) Differential transmit signal to port 2 magnetics
P2_TXREF	59	Analog output	Port 2 transmitter current setting pin, grounded extemally
P3_RXIP	73	Analog input	(+) Differential receive signal from port 3 magnetics
P3_RXIN	74	Analog input	(−) Differential receive signal from port 3 magnetics
P3_TXOP	66	Analog output	(+) Differential transmit signal to port 3 magnetics
P3_TXON	67	Analog output	(−) Differential transmit signal to port 3 magnetics
P3_TXREF	70	Analog output	Port 3 transmitter current setting pin, grounded extemally

Table 4

Expansion Port

Signal	Pin no.	Type	Description
IRD4 IRD3 IRD2 IRD1 IRD0	1 128 127 98 97	High drive open drain digital output and digital input with pull-up	**Inter-repeater data**. Transfers 5-bit symbol data between NWK954s on the local expansion bus, and to/from the backplane drivers. Transfers are synchronous to BPCLK.Require external pull-ups for correct operation.
LACTOUT_N	2	High drive digital output	**Local activity output**. Indicates receive activity in this NWK954. Connects to all other NWK954s on the local expansion bus. Output changes asynchronously.
LACTIN_N5 LACTIN_N4 LACTIN_N3 LACTIN_N2 LACTIN_N1	10 9 8 7 6	Digital input, no pull-up	**Local activity inputs**. One input from each NWK954 on the local expansion bus to indicate receive activity. Unused inputs must be pulled high or connected directly to DIGVDD. Inputs are sampled on on the rising edge of TXCLKIN.
BPACTOUT_N	105	Standard digital output	**Backplane activity output.** Indicates receive activity on any of the NWK954s on the local expansion bus. Drives the backplane through an external driver. Only one of the local NWK954s is required to drive this signal, the others should be left unconnected. Output changes asynchronously.

Table 5

Continues…

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Expansion Port (Continued)

Signal	Pin no.	Type	Description
BPACTIN_N7 BPACTIN_N6 BPACTIN_N5 BPACTIN_N4 BPACTIN_N3 BPACTIN_N2 BPACTIN_N1	89 90 91 92 101 102 103	Digital input, no pull-up	**Backplane activity inputs.** Indicate activity on up to 7 other hubs connected to the backplane. Received from the backplane via external receivers. Each NWK954 connected to the local expansion bus receives all of these backplane activity inputs. Unused inputs must be pulled high or connected directly to DIGVDD. Inputs are sampled on the rising edge of TXCLKIN.
BPDIE_N	107	Standard digital output and digital input with pull-up	**Backplane data input enable.** Enables the external receivers that pass backplane data and clock onto the local IRD[4:0] and BPCLK lines. Only one of the local NWK954s is required to drive this signal, the others should be left unconnected. This signal changes asynchronously. Polarity defaults to active low but may be switched to active high by adding an external 10kΩ pull-down.
BPDOE_N	108	Standard digital output and digital input with pull-up	**Backplane data output enable.** Enables the external drivers that pass the local IRD[4:0] and BPCLK signals onto the backplane. Output changes on the rising edge of TXCLKIN. Only one of the local NWK954s is required to drive this signal, the others should be left unconnected. Polarity defaults to active low but may be switched to active high by adding an external 10kΩ pull-down.
BPCLK	96	High drive open drain digital output and digital input with pull-up	**25MHz backplane clock.** Data transitions on IRD[4:0] are synchronised to this clock. When another hub in the stack is sourcing data, this clock is received from the backplane to all local NWK954s through an external receiver. When a local NWK954 is sourcing data, BPCLK is supplied to the backplane through an external driver. Requires external pull-up for correct operation
BPCOL_N	95	High drive open drain digital output and digital input with pull-up	**Backplane collision.** This signal may be driven by any of the local NWK954s to indicate that a collision has been detected, and is supplied to the backplane through an external driver. Output transitions are synchronous to the rising edge of TXCLKIN and the input is sampled on the rising edge of TXCLKIN. Requires external pull-up for correct operation.
BPCOLIN_N	104	Digital input, no pull-up	**Backplane collision input.** Indicates that a collision has been detected by any hub in the stack. Received from the backplane via an external receiver. Connects to all local NWK954s. Must be pulled high or connected directly to DIGVDD if not used. Input is sampled on the falling edge of TXCLKIN.
BPCOLOE_N	106	Standard digital output and digital input with pull-up	**Backplane collision output enable.** Enables the external driver that passes BPCOL_N onto the backplane. Only one of the local NWK954s is required to drive this signal, the others should be left unconnected. Output changes on the rising edge of TXCLKIN. Polarity defaults to active low but may be switched to active high by adding an external 10kΩ pull-down.

Table 5 (continued)

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LED Drivers

Signal	Pin no.	Type	Description
COLLED_N	109	Standard digital output	**Collision LED.** Drives an LED to indicate that a collision has occurred either locally or elsewhere in the stack.
P0_RXLED_N	124	Standard digital output	**Port 0 activity LED.** Drives an LED to indicate link/activity on port 0. The LED is turned on when a link is established and flashes off when a packet is being received.
P1_RXLED_N	122	Standard digital output	**Port 1 activity LED.** Drives an LED to indicate link/activity on port 1. The LED is turned on when a link is established and flashes off when a packet is being received.
P2_RXLED_N	120	Standard digital output	**Port 2 actlvlty LED.** Drives an LED to indicate link/activity on port 2. The LED is turned on when a link is established and flashes off when a packet is being received.
P3_RXLED_N	118	Standard digital output	**Port 3 activlty LED.** Drives an LED to indicate link/activity on port 3. The LED is turned on when a link is established and flashes off when a packet is being received.
P0_ERLED_N	123	Standard digital output	**Port 0 error LED.** Drives an LED to indicate an error on port 0. See the text for a full description.
P1_ERLED_N	121	Standard digital output	**Port 1 error LED.** Drives an LED to indicate an error on port 1. See the text for a full description.
P2_ERLED_N	119	Standard digital output	**Port 2 error LED.** Drives an LED to indicate an error on port 2. See the text for a full description.
P3_ERLED_N	117	Standard digital output	**Port 3 error LED.** Drives an LED to indicate an error on port 3. See the text for a full description.
ACTLED_N4 ACTLED_N3 ACTLED_N2 ACTLED_N1 ACTLED_N0	116 115 114 113 112	Standard digital outputs	**Utilization LEDs.** Drives 5 LEDs to indicate utilization of the network segment. See the text for a full description.

Table 6

Clocks and Controls

Signal	Pin no.	Type	Description
TXCLKIN	86	Digital input no pull-up	**25MHz reference clock.** Supplied from an external source to all NWK954s on the local expansion bus.
RESET_N	5	Open drain digital output and digital input, no pull-up	Asynchronous reset. This signal is driven low by the on-chip power-on reset circuit, but may also be driven low externally for manual reset. Must be pulled high by an external 5kΩ resistor.
PSEN0 PSEN1	87 88	Digital inputs with pull-ups	**Power-savlng enables.** 11 enables power-saving on all ports. 01 suppresses power saving on port 0, 10 suppresses power saving on port 3, 00 suppresses power-saving on all ports.
TA4 TA3 TA2	13 14 15	Digital inputs, no pull-ups	**Scrambler seed.** Each ot the four PHY modules in the NWK954 is provided with a unique scrambler seed derived from TA[4:2]. To ensure that all ot the local PHYs have unique scrambler seeds, each NWK954 connected to the local expansion bus should have its TA[4:2] input set to a unique value by connecting to DIGVDD or DIGGND.

Table 7

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Power

Signal	Pin no.	Type	Description
DIGGND[5: 1]	94, 100, 111, 126, 4	Ground	Digital ground
DIGVDD[5: 1]	93, 99, 110, 125, 3	Power	Digital power
DIGGND6	85	Ground	Quiet digital ground
DIGVDD6	84	Power	Quiet digital power
SUBVDD[2:1]	81, 16	Power	Substrate power
VREFGND	83	Ground	Voltage reference ground
VREFVDD	82	Power	Voltage reference power
P0_TXGND[3:1]	26, 28, 32	Ground	Transmit ground for port 0
P0_TXVDD[3:2]	25, 29	Power	Transmit power for port 0
P0_RXGND[3:1]	17, 20, 21	Ground	Receive ground for port 0
P0_RXVDD[3:1]	18, 19,22	Power	Receive power for port 0
P1_TXGND[3:1]	39, 37, 33	Ground	Transmit ground for port 1
P1_TXVDD[3:2]	40, 36	Power	Transmit power for port 1
P1_RXGND[3:1]	48, 45, 44	Ground	Receive ground for port 1
P1_RXVDD[3:1]	47, 46,43	Power	Receive power for port 1
P2_TXGND[3:1]	58, 60, 64	Ground	Transmit ground for port 2
P2_TXVDD[3:2]	57, 61	Power	Transmit power for port 2
P2_RXGND[3:1]	49, 52, 53	Ground	Receive ground for port 2
P2_RXVDD[3:1]	50, 51, 54	Power	Receive power for port 2
P3_TXGND[3:1]	71, 69, 65	Ground	Transmit ground for port 3
P3_TXVDD[3:2]	72, 68	Power	Transmit power for port 3
P3_RXGND[3:1]	80, 77,76	Ground	Receive ground for port 3
P3_RXVDD[3:1]	79, 78, 75	Power	Receive power for port 3

Table 8

No Connects

Signal	Pin no.	Type	Description
TDC	11	Factory test	**Do not connect to this pin**
TDIO	12	Factory test	**Do not connect to this pin**

Table 9

ABSOLUTE MAXIMUM RATINGS

Exceeding the Absolute Maximum Ratings may cause permanent damage to the device. Extended exposure at these ratings will affect device reliability.

Supply voltage, V_{DD}	0·5V to ¯7·0V
Input voltage	0·5V to V_{DD} ¯0·5V
Output voltage	0·5V to V_{DD} ¯0·5V
Static discharge voltage	4KV HBM
Storage temperature, T_S	40°C to +125°C

RECOMMENDED OPERATING CONDITIONS

Neither performance nor reliability are guaranteed outside these limits. Extended operation outside these limits may affect device reliability.

Supply voltage, V_{DD}	¯5·0V ± 5%
Input voltage	0V to V_{DD}
Output voltage	0V to V_{DD}
Current per pin	100mA
Ambient temperature, T_A	0°C to ¯70°C

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POWER SUPPLY

Recommended Operating Conditions apply except where otherwise stated

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage	V_{DD}	4·25		5·25	V	
Supply current	I_{DD}			400	mA	Includes current through external components(see Fig. 8)

DC ELECTRICAL CHARACTERISTICS

Recommended Operating Conditions apply except where otherwise stated

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Digital input, no pull-up						
Input high voltage	V_{IH}	2		V_{DD}	V	
Input low voltage	V_{IL}	V_{SS}		0·8	V	
Hysteresis	V_H	0·3			V	
Input high current	I_{IH}			1	µA	
Input low current	I_{IL}			1	µA	
Capacitance	C_I			8	pF	Including package
Digital input, with pull-up						
Input high voltage	V_{IH}	2		V_{DD}	V	
Input low voltage	V_{IL}	V_{SS}		0·8	V	
Hysteresis	V_H	0·3			V	
Input high current	I_{IH}			1	µA	
Input low current	I_{IL}	17		130	µA	V_{IL} = 0
Capacitance	C_I			8	pF	Including package
Standard digital output						
Output high voltage	V_{OH}	4		V_{DD}	V	I_{OH} = 6mA
Output low voltage	V_{OL}	V_{SS}		0·4	V	I_{OL} = 6mA
Rise time	t_R			4	ns	0·4V to 2·4V into 20pF load
Fall time	t_F			3	ns	2·4V to 0·4V into 20pF load
Tristate leakage		1		1	µA	
Capacitance	C_O			8	pF	Including package
High drive digital output						
Output high voltage	V_{OH}	4		V_{DD}	V	I_{OH} = 24mA
Output low voltage	V_{OL}	V_{SS}		0·4	V	I_{OL} = 24mA
Rise time	t_R			TBD	ns	0·4V to 2·4V into 100pF load
Fall time	t_F			TBD	ns	2·4V to 0·4V into 100pF load
Tristate leakage		1		1	µA	
Capacitance	C_O			8	pF	Including package
Open drain digital output						
Output low voltage	V_{OL}	V_{SS}		0·4	V	I_{OL} = 6mA
Fall time	t_F			TBD	ns	5V to 0·4V into 30pF load
Tristate leakage		1		1	µA	
Capacitance	C_O			8	pF	Including package
High drive open drain digital output						
Output low voltage	V_{OL}	V_{SS}		0·4	V	I_{OL} = 24mA
Fall time	t_F			TBD	ns	2·4V to 0·4V into 100pF load
Tristate leakage		1		1	µA	
Capacitance	C_O			8	pF	Including package

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AC ELECTRICAL CHARACTERISTICS

Recommended Operating Conditions apply except where otherwise stated

TXCLK and RESET_N

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
TXCLKIN Frequency Duty cycle	f_{TCLK}	 45	25 ± 100ppm	 55	MHz %	
RESET_N Pulse width	t_{WRES}	100	-	-	ns	

TXOP/TXON

Characteristic	Reference
The differential output voltage shall be in the range 950mV to 1050mV.	TP-PMD 9.1.2.2
The differential overshoot shall not exceed 5%.	TP-PMD 9.1.3
Overshoot transients must decay to within 1% of the steady state voltage within 8ns of the start of the differential signal transition.	TP-PMD 9.1.3
The signal amplitude symmetry shall be in the range 98% to 102%.	TP-PMD 9.1.4
The return loss shall be greater than 16dB from 2MHz to 30MHz.	TP-PMD 9.1.5
The return loss shall be greater than 16-20 log(f/30MHz)dB from 30MHz to 60MHz	TP-PMD 9.1.5
The return loss shall be greater than 10dB from 60MHz to 80MHz.	TP-PMD 9.1.5
The rise and fall times measured from 10% to 90% of the steady state output voltage shall be between 3ns and 5ns.	TP-PMD 9.1.6
Difference between max. and min. rise and fall times shall be less than 0·5ns.	TP-PMD 9.1.6
Duty cycle distortion must be less than ±0·25ns measured at 50% of the steady state output voltage for a data sequence of 01010101 (NRZ)	TP-PMD 9.1.8
Total transmit jitter, including duty cycle distortion and baseline wander, must be less than 1·4ns p-p	TP-PMD 9.1.9

RXIP/RXIN

Characteristic	Reference
The return loss shall be greater than 16dB from 2MHz to 30MHz.	TP-PMD 9.2.2
The retum loss shall be greater than 16-20 log(f/30MHz)dB from 30MHz to 60MHz.	TP-PMD 9.2.2
The return loss shall be greater than 10dB from 60MHz to 80MHz	TP-PMD 9.2.2

EXTERNAL COMPONENTS (See Fig. 8)

Component	Value	Tol.	Description
R1	16·2Ω	1%	Receiver impedance matching resistor network.
R2	34·0Ω	1%	Receiver impedance matching resistor network.
R3	50Ω	1%	Transmitter load resistors.
R4	1·2kΩ	1%	Sets the transmitter output current.
R5	5kΩ	5%	This resistor is required even if the RESET_N signal is not used externally.
R6	10kΩ	5%	Optional pull-downs on backplane enable signals. These outputs are normally active low. Each output can be independently changed to active high by the addition of this resistor.
R7	200Ω min*	5%	Pull-ups required on open drain expansion port outputs.
R8			Series resistors. May be required in some applications where the expansion ports are used.*
C1, C3	0·01µF		
C2	0·1µF		

* Refer to Mitel

Table 10

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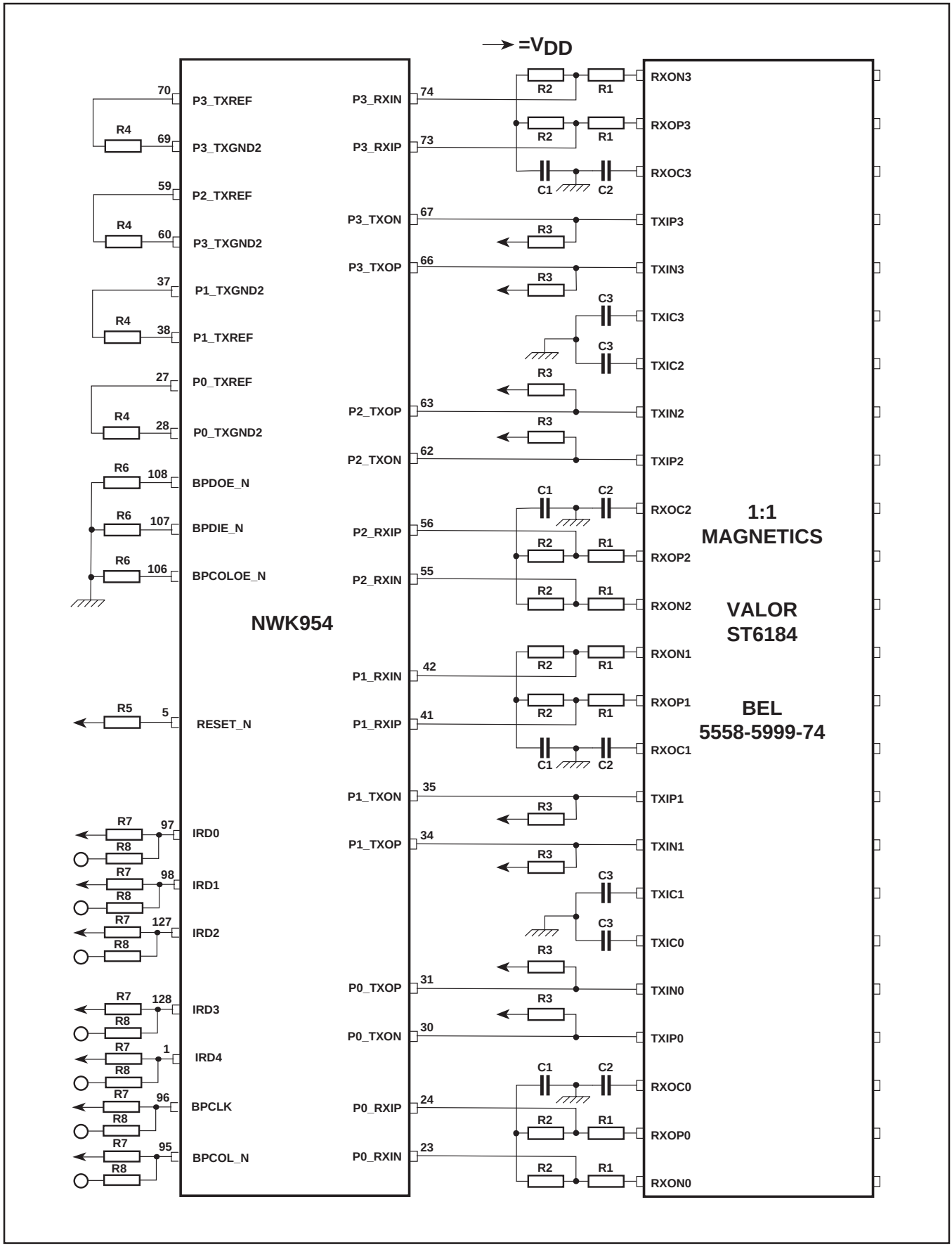

Fig. 8 External components

For further details on magnetics please refer to vendor.

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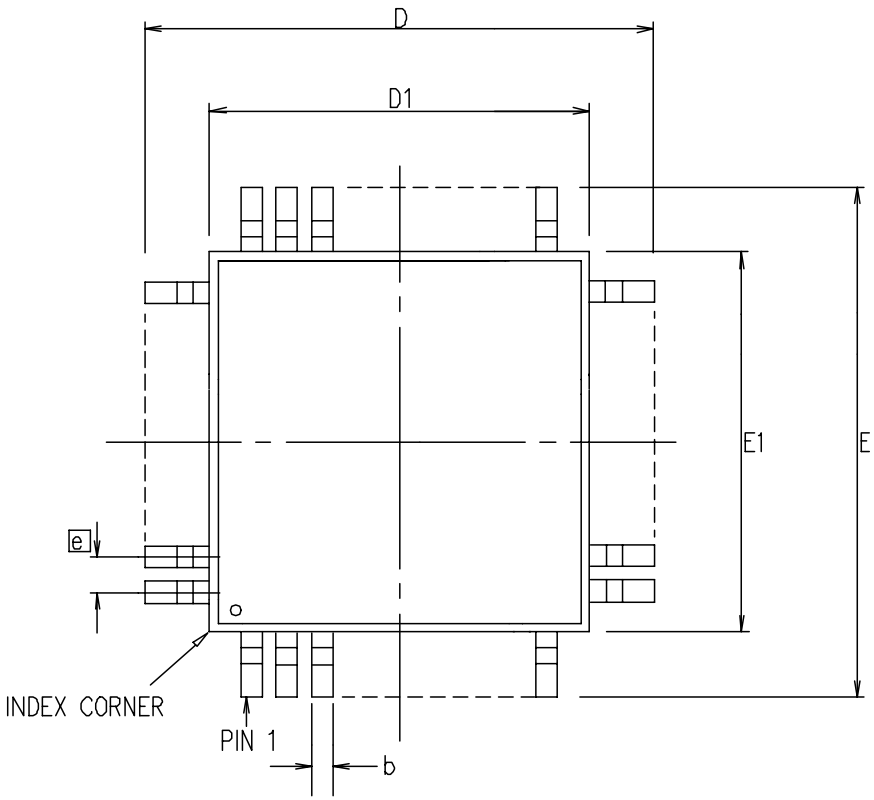

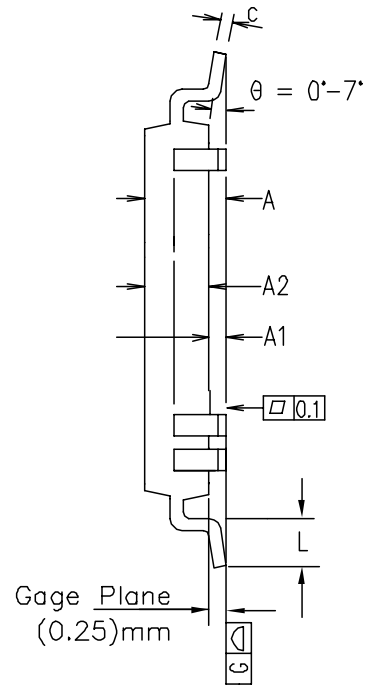

Symbol	Control Dimensions in millimetres			Altern. Dimensions in inches	
	MIN	MAX		MIN	MAX
A	–	4.10		–	0.161
A1	0.25	0.50		0.010	0.020
A2	3.20	3.60		0.126	0.142
D	31.20 BSC			1.228 BSC	
D1	28.00 BSC			1.102 BSC	
E	31.20 BSC			1.228 BSC	
E1	28.00 BSC			1.102 BSC	
L	0.73	1.03		0.029	0.041
e	0.80 BSC.			0.031 BSC.	
b	0.29	0.45		0.011	0.018
c	0.11	0.23		0.004	0.009
	Pin features				
N	128				
ND	32				
NE	32				
NOTE	SQUARE				

Conforms to JEDEC MS-022 DB Iss. B

Notes:

1. Pin 1 indicator may be a corner chamfer, dot or both.
2. Controlling dimensions are in millimeters.
3. The top package body size may be smaller than the bottom package body size by a max. of 0.15 mm.
4. Dimension D1 and E1 do not include mould protusion.
5. Dimension b does not include dambar protusion.
6. Coplanarity, measured at seating plane G, to be 0.010 mm max.

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MITEL SEMICONDUCTOR

Title: Package Outline Drawing for 128L MQFP (GP) (28x28x3.4) mm, Body+3.2 mm

Drawing Number

GPD00301

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